Elixir-SV SystemVerilog Testsuite Datasheet

Introduction

The Elixir-SV is a comprehensive SystemVerilog Test Suite developed by VerifWorks (http://www.verifworks.com), a CVC venture. It is aimed at slashing validation time for EDA vendors by assisting in their tool development cycle. It also enables the semiconductor design teams (and/or CAD teams) to qualify and evaluate competing EDA tools thereby avoiding costly redesigns and re-spins. Overall from a management perspective Elixir-SV dramatically reduces our customers' validation effort, costs and time-to-market. SV Test Suite addresses the needs of EDA tool developers to quickly measure the quality of their products. Elixir-SV is a comprehensive test suite based on SystemVerilog IEEE 1800-2005 standard. It is also being upgraded to include SystemVerilog IEEE 1800-2009 and 1800-2012 revisions based on customer demand. Incorporation of these standards in the design cycle will enable semiconductor design teams to create solutions that make designers more efficient.

Our Elixir-SV Test Suite gives EDA tool developers an opportunity to characterize EDA tools for Design features, randomization, constraint, coverage and assertions constructs in SystemVerilog language. This also enables to discover the language and RTL non-compliance early in the product development and product validation life cycle.

Elixir-SV Test Suite highlights:

- The comprehensive and robust nature of this test suite reduces the PV (Product Validation) development costs and time-to-market for EDA products
- Provides an unbiased quality analysis of EDA tools for semiconductor design houses and their CAD teams.
- Encourages development of standard-based products
- Well organized test cases leading to precise evaluation of bugs and errors in the product
- This test suite thoroughly measures the product quality and gives an unbiased feedback on product quality for EDA tool developers.

Features of SV Test Suite

- **Comprehensive SV Test Suite**

  These test cases are well organized which enables users to evaluate syntax, semantics, synthesizability, and simulation aspects of a SystemVerilog supported EDA tool.

- **Syntax and Semantics Cover**

  Includes over 720 test cases that cover constructs, styles for both Design and Verification support.

Scenarios/Chapters	**No. Of Test cases**
Data Types	43
Aggregate Data Types	15
Process	14
Assignment Statements	28
Operators & Expressions	39
Procedural Programming Statement	126
Tasks & Subroutines	8
Interfaces	5
Packages	6
UDPs	7
Protect Envelops	2
Compiler Directives	21
Modules & Hierarchy	59
Generate Blocks	20
System tasks & Functions	2
Classes	27
Process	45
Assignment Statements	17
Operators	14
Clocking Blocks	16
Assertions	68
Constrained Random Verification	96
Functional Coverage	53
DPI	12
Total	**720**

- **Well Documented Test Plans**

  The test plans describe all test objectives and are categorized by sections. Each test case has a reference to the section number of the test plan.

- **Test Benches and Reference Golden**

  Provides test benches to instantiate test cases and apply vectors on inputs. Outputs are captured after an appropriate interval and written on to a file. Test bench can be easily applied to the test tool and compare the outputs.

- **Highlights**

  a. Over 720 test cases along with test benches

     i. Design Constructs: 348 test cases
     ii. Test bench features: 372 test cases

  b. Golden output for comparison.

  c. Detailed test plans with cross-reference to test cases.

  d. Well-organized test cases highlighting testing objectives.

  e. Both positive and negative test cases.

Roadmap

We continue to add more features to this product such as:

- More tests
- Synthesis subset
- Formal Verification sub-set
- New language consutrcyts support