APB MIP DATASHEET

Intended Use:

- ✓ To monitor protocol signals
- ✓ To validate behavior of design
- ✓ To identify test bench holes

Key Features:

- ✓ Supports multi slave configuration
- ✓ Allows White box level verification of signals

Benefits:

- ✓ Protocol violations will be displayed
- ✓ Hunting bugs easily

Simulation Support:

MIP is developed & simulated in RIVIERA simulation tool from ALDEC.

Contents:

General Description:

MIP stands for Monitor Intellectual Property which is designed to monitor Advanced Peripheral Bus (APB) signals. MIP is modeled using SystemVerilog Assertions. It includes both assert & cover properties. Cover directive acts as a monitor where as an assert directive acts as a checker. Hence assert directives are used to identify design bugs or protocol violations & cover directives are used to identify test bench holes. This MIP provides various properties to cover & assert enabling users to corner bugs.

Assertions & Cover List:

In Master:

There are 12 assert directives & 28 cover directives in master MIP.

In Slave:

There are 04 assert directives & 13 cover directives in slave MIP.

Note:

Some assert directives & cover directives will be common to both master & slave MIP.

Binding:

Binding the MIP to the design is done through “bind” construct in SystemVerilog Assertions.

Block Diagram: